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RISC-V-based System-on-Chips for IoT Applications

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I. INTRODUCTION

The rapidly growing IoT devices pose challenges to power requirements. Traditional power sources, such as batteries, face many limitations, especially regarding durability. By gathering energy from environmental sources, power harvesting promises the future of a fully connected world. Achieving ultralow-voltage operation for direct powering from harvesters involves specific strategies. This necessity gives rise to circuit solutions characterized by low minimum operating voltages, power consumption in the pW range, and resilience against supply fluctuations. This work provides a combined solution to achieve the low-power, low-area target for pure power-harvesting devices: a minimal resource RISC-V processor with ultra-low power, low leakage ASIC technology. We implemented two serial architecture-based RISC-V SoCs, SERV-32I and SERV-32E, on 65-nm SOTB technology. The SERV-32I is a basic implementation of the RISC-V base specification, while the SER-32E implements the embedded specification with 16 registers truncated in the Register File. The lowest power consumption achieved by SERV-32I and SERV-32E is reported at 34nW and 9.7nW with a 0.27V power supply and frequency of 7kHz and 3kHz at VDD = 0.27V, respectively. The SERV-32E processor's footprint is about 28% smaller than the SERV-32I's, while performance only drops by about 5%, with the SERV-32E achieving Dhrystone results of 1.05 DMIPS/MHz and SERV-32I at 1.11 DMIPS/MHz at 50MHz.

II . PROPOSED ARCHITECTURE

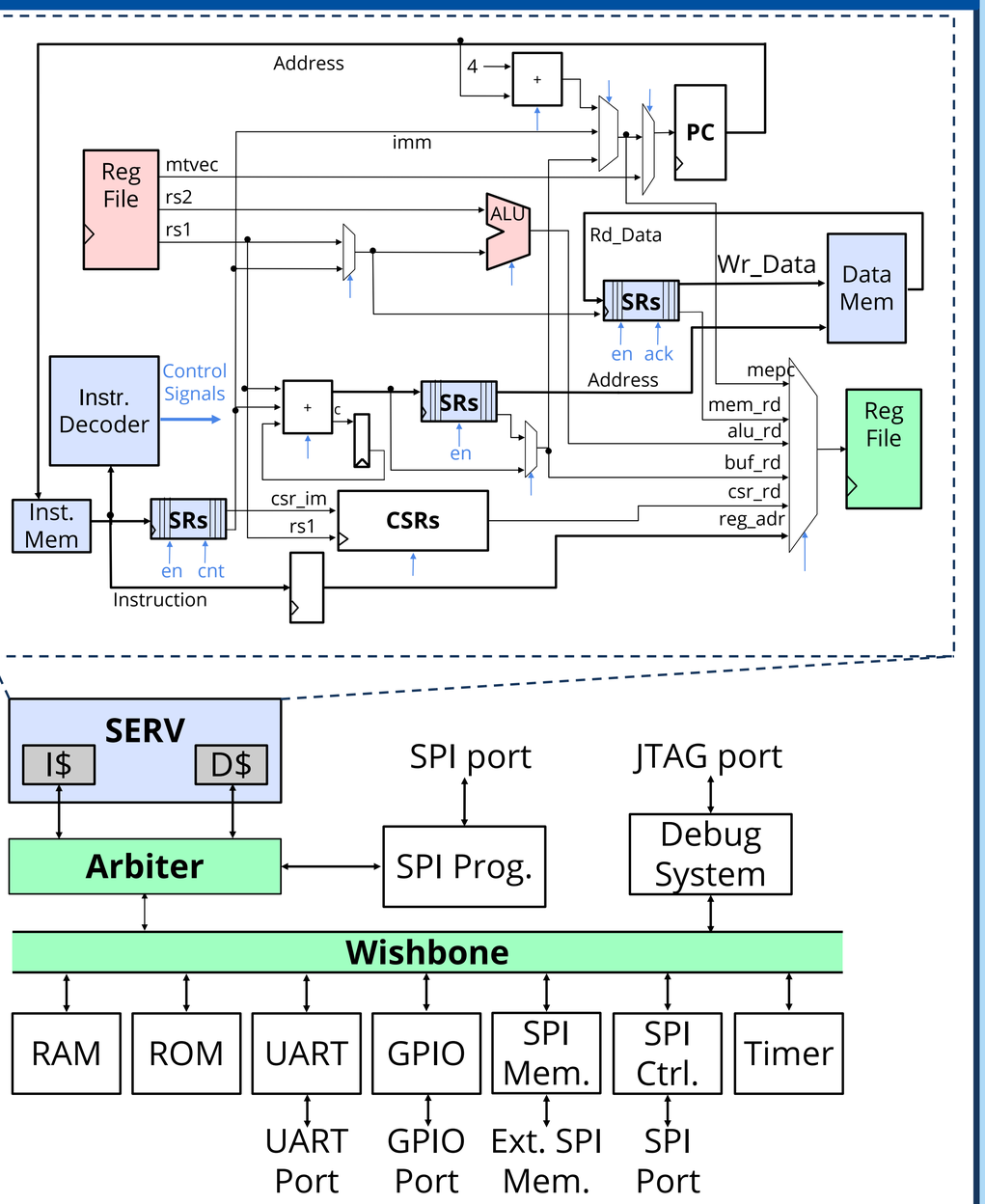

***Fig. 1*:** SERV System on Chip

III . CHIP MICROGRAPH

VDD:0.27V~1.2V VBB: -2.0V~2.0V	Operating Voltage	VDD:0.27V~1.2V VBB: -2.0V~2.0V
98,423	Area[µm2]	118,026
~70,000	Gate Count	~84,000
11kHz~30MHz	Operating Frequency	10kHz~30MHz
VDD: 0.27V ~ 1.1V VBB: -2.0V ~ -0.4V	Sub-µW Operating	VDD: 0.27V ~ 0.9V VBB: -2.0V ~ -0.4V
SERV-32E	Microprocessor	SERV-32I

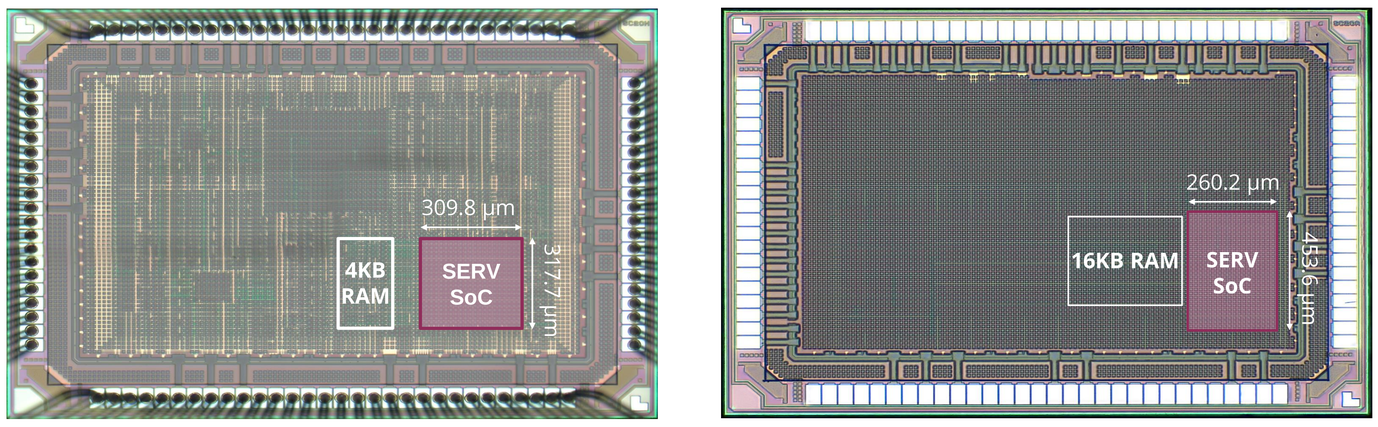

***Fig. 2*:** SERV SoCs Micrograph.

Table I. ASIC Implementation in comparison.

	Tech.	VDD [V]	Energy [µW/MHz]	Leakage [µW]	NAND Gate	Freq. [MHz]
COOL Chips'14 [1]	SOTB 65nm	0.22	13.3	0.049	50.1k	14
TCAS-I'20 [2]	FDX 22nm	0.42	4.47	105.4	-	18
COOL Chips'20[3]	FDX 22nm	0.55	6.3	6.6	-	40
JSSCC'21[4]	FDSOI 28nm	0.4	3.3	8.4	-	40
SSC-L'21 [5]	FDSOI 65nm	0.5	13.4	-	-	0.00207
SERV-32E	SOTB 65nm	0.29	2.37	0.0024	-	0.01
SERV-32E SoC	SOTB 65nm	0.27	3.11	0.0037	70k	0.01

IV . MEASUREMENT RESULTS

SERV-32I and SERV-32 are compared side-by-side in terms of power per cycle, power consumption, and area distribution. They are also compared with other state-of the-art implementations. The SERV-32E's energy is the lowest of all the implementations compared.

***Fig. 3*:** SERV SoCs Power breakdown at frequency of 32kHz, VDD = 0.4V and different bias voltage

***Fig. 4*:** SERV Active Energy efficiency at VBB = -0.8V and different VDD

***Fig. 5*:** Area distribution of SoCs

REFERENCES

[1] K. Ishibashi *et al.*, "A Perpetuum Mobile 32bit CPU with 13.4pJ/cycle, 0.14µA sleep current using Reverse Body Bias Assisted 65nm SOTB CMOS technology," COOL Chips, 2014.
[2] A. D. Mauro *et al.*, "Always-On 674µ W@4GOP/s Error Resilient Binary Neural Networks With Aggressive SRAM Voltage Scaling on a 22-nm IoT End-Node," TCAS-I, 2020.
[3] D. Walter *et al.*, "A 0.55V 6.3uW/MHz Arm Cortex-M4 MCU with Adaptive Reverse Body Bias and Single Rail SRAM," COOL Chips, 2020.
[4] D. Bol *et al.*, "SleepRunner: A 28-nm FDSOI ULP Cortex-M0 MCU With ULL SRAM and UFBR PVT Compensation for 2.6-3.6-µW/DMIPS 40-80-MHz Active Mode and 131-nW/kB Fully Retentive Deep-Sleep Mode," JSSC, 2021.
[5] D. S. Truesdell et al.,"A 6–140-nW 11Hz–8.2-kHz DVFS RISC-V Microprocessor Using Scalable Dynamic Leakage-Suppression Logic," SSC-L, 2021.

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